What is claimed is:

1. A method comprising:

propagating a first loop condition of a hardware loop via a first pipeline of a pipelined processor; and

propagating a second loop condition via a second pipeline of the pipelined processor.

2. The method of claim 1, further comprising:

writing the loop conditions to a first set of registers prior to propagating the loop conditions, and

writing the loop conditions to a second set or registers after propagating the loop conditions.

3. The method of claim 1, wherein the first and second loop conditions are propagated in parallel.

4. A method of claim 1, further comprising propagating a third loop condition via a third pipeline.

5. The method of claim 2, further comprising generating the loop conditions of the hardware loop prior to writing the loop conditions to the first set of registers.

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6. The method of claim 5, wherein generating the loop conditions comprise calculating at least one of the loop conditions from program counter relative data in a loop setup instruction.

7. A method comprising:

calculating a first loop condition of a hardware loop from a loop setup instruction using a first arithmetic logic unit in a first pipeline; and

calculating a second loop condition of the hardware loop from the loop setup instruction using a second arithmetic logic unit in a second pipeline.

8. The method of claim 7, further comprising writing the first and second loop conditions to a first set of registers.

9. The method of claim 7, further comprising:

calculating a third loop condition of the hardware loop from the loop setup instruction using a third arithmetic logic unit in a third pipeline; and

writing the first, second and third loop conditions to a first set of registers.

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10. The method of claim 7, wherein calculating the first loop condition and calculating the second loop condition occur in parallel.

11. The method of claim 8, further comprising propagating the first loop condition to a second set of registers via a first pipeline.

12. The method of claim 11, further comprising propagating the second loop condition to the second set of registers via a second pipeline.

13. An apparatus comprising:

a first pipeline including a first arithmetic logic unit and a second pipeline including a second arithmetic logic unit, and

a control unit coupled to the pipelines, the control unit adapted to:

calculate a first loop condition of a hardware loop from a loop setup instruction using the first arithmetic logic unit in the first pipeline; and

calculate a second loop condition of the hardware loop from a loop setup instruction using the second arithmetic logic unit in the second pipeline.

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14. The apparatus of claim 13, the apparatus further comprising a first set of registers coupled to the control unit, wherein the control unit is further adapted to write the first and second loop conditions of the hardware loop to the first set of registers.

15. The apparatus of claim 14, the apparatus further comprising a third pipeline coupled to the control unit, the third pipeline including a third arithmetic logic unit, the control unit further adapted to:

calculate a third loop condition of the hardware loop from the loop setup instruction using the third arithmetic logic unit in the third pipeline; and

write the first, second and third loop conditions of the hardware loop to the first set of registers.

16. The apparatus of claim 14, the apparatus further comprising a second set of registers coupled to the control unit, wherein the control unit is further adapted to propagate at least one of the loop conditions to the second set of registers via the first pipeline.

17. The apparatus of claim 16, the control unit further adapted to propagate at least one of the loop conditions to the second set of registers via the second pipeline.

18. The apparatus of claim 15, the apparatus further comprising a second set of registers coupled to the control unit, the control unit further adapted to:

propagate at least one of the loop conditions to the second set of registers via the first pipeline;

propagate at least one of the loop conditions to the second set of registers via the second pipeline; and

propagate at least one of the loop conditions to the second set of registers via the third pipeline.

19. The apparatus of claim 14, wherein the first set of registers are speculative registers.

20. The apparatus of claim 13, wherein at least one of the pipelines is a data address generation pipeline.

21. The apparatus of claim 13, wherein at least one of the pipelines is a system pipeline.

22. An apparatus comprising a set of registers, a first pipeline, and a second pipeline; and

a control unit coupled to the set of registers, the first pipeline and the second pipeline, the control unit adapted to:

propagate at least one loop condition of a hardware loop to the set of registers via the first pipeline; and

propagate at least one loop condition of the hardware loop to the set of registers via the second pipeline.

23. The apparatus of claim 22, wherein the set of registers are a second set of registers, the apparatus further including a first set of registers coupled to the control unit, wherein the control unit is further adapted to:

write the loop conditions of the hardware loop to the first set of registers prior to propagating at least one of the loop conditions to the second set of registers.

24. The apparatus of claim 22, wherein at least one of the pipelines is a data address generation pipeline.

25. The apparatus of claim 22, wherein at least one of the pipelines is a system pipeline.

26. A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a first pipeline, a second pipeline, and a control unit adapted to:

calculate a first loop condition of a hardware loop from a loop setup instruction using a first arithmetic logic unit in the first pipeline,

calculate a second loop condition of the hardware loop from the loop setup instruction using a second arithmetic logic unit in the second pipeline; and

write the first and second loop conditions of the hardware loop to the first set of registers.

27. The system of claim 26, the processor including a third pipeline, the control unit further adapted to:

calculate a third loop condition of the hardware loop from the loop setup instruction using a third arithmetic logic unit in the third pipeline; and

write the first, second and third loop conditions of the hardware loop to the first set of registers.

28. A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a second set of registers, a first pipeline, a second pipeline, and a control unit adapted to:

write loop conditions of a hardware loop to the first set of registers;

propagate at least one of the loop conditions to the second set of registers via the first pipeline; and

propagate at least one of the loop conditions to the second set of registers via the second pipeline.

29. The system of claim 28, the processor further including a third pipeline, the control unit further adapted to propagate at least one of the loop conditions to the second set of registers via the third pipeline.

30. The system of claim 28, the control unit further adapted to:

calculate a first loop condition of the hardware loop from a loop setup instruction using a first arithmetic logic unit in the first pipeline; and

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calculate a second loop condition of the hardware loop from the loop setup instruction using a second arithmetic logic unit in the second pipeline.